Amendments to the Claims

This listing of the Claims will replace all prior versions and listings of the claims in this patent application.

Listing of the Claims

1-93. (canceled)

94. (new) A semiconductor chip or wafer comprising:

a semiconductor substrate having multiple semiconductor devices;

an interconnecting metallization structure over said semiconductor substrate;

a passivation layer over said interconnecting metallization structure; and

an upper metallization structure over said passivation layer and comprising gold, wherein said upper metallization structure comprises a connecting portion connecting multiple portions of said interconnecting metallization structure.

95. (new) The semiconductor chip or wafer of claim 94, wherein said passivation layer comprises a topmost nitride layer of said semiconductor chip or wafer.

96. (new) The semiconductor chip or wafer of claim 94, wherein said passivation layer comprises a topmost oxide layer of said semiconductor chip or wafer.

97. (new) The semiconductor chip or wafer of claim 94, wherein said passivation layer comprises a topmost insulation layer, formed using a CVD process, of said semiconductor chip or wafer.

98. (new) The semiconductor chip or wafer of claim 94, wherein said interconnecting metallization structure comprises a first contact pad exposed by an opening in said passivation layer, and said upper metallization structure comprises a second contact pad connected to said first contact pad, wherein the positions of said first and second contact pads from a top view are different.

99. (new) The semiconductor chip or wafer of claim 94, wherein said gold comprises a gold layer having a thickness of between 2 and 100 μm.

100. (new) The semiconductor chip or wafer of claim 99, wherein said upper metallization structure further comprises a metal layer under said gold layer, wherein said metal layer comprises titanium tungsten.

101. (new) The semiconductor chip or wafer of claim 94, wherein said semiconductor substrate comprises silicon.

102. (new) The semiconductor chip or wafer of claim 94 further comprising a topmost polymer layer over said passivation layer, wherein said upper metallization structure comprises an upper metal layer over said topmost polymer layer.

103. (new) The semiconductor chip or wafer of claim 94, wherein said interconnecting metallization structure comprises electroplated copper.

104. (new) The semiconductor chip or wafer of claim 94, wherein said interconnecting metallization structure comprises aluminum.

105. (new) The semiconductor chip or wafer of claim 94, wherein said upper metallization structure comprises an electroplated metal.

106. (new) A semiconductor chip or wafer comprising:

a semiconductor substrate having multiple semiconductor devices;

an interconnecting metallization structure over said semiconductor substrate and comprising a first contact pad;

a passivation layer over said interconnecting metallization structure, wherein said first contact pad is exposed by an opening in said passivation layer; and

an upper metallization structure over said passivation layer and comprising a gold layer with a thickness of between 2 and 100 μm, wherein said upper metallization structure comprises a second contact pad connected to said first contact pad, and wherein the positions of said first and second contact pads from a top view are different.

107. (new) The semiconductor chip or wafer of claim 106, wherein said passivation layer comprises a topmost nitride layer of said semiconductor chip or wafer.

108. (new) The semiconductor chip or wafer of claim 106, wherein said passivation layer comprises a topmost oxide layer of said semiconductor chip or wafer.

109. (new) The semiconductor chip or wafer of claim 106, wherein said passivation layer comprises a topmost insulation layer, formed using a CVD process, of said semiconductor chip or wafer.

110. (new) The semiconductor chip or wafer of claim 106, wherein said upper metallization structure further comprises a metal layer under said gold layer, wherein said metal layer comprises titanium tungsten.

111. (new) The semiconductor chip or wafer of claim 106, wherein said semiconductor substrate comprises silicon.

112. (new) The semiconductor chip or wafer of claim 106, wherein said second contact pad is used to be wirebonded thereto.

113. (new) The semiconductor chip or wafer of claim 106 further comprising a wirebond connected to said second contact pad.

114. (new) The semiconductor chip or wafer of claim 106 further comprising a metal bump formed on said second contact pad.

115. (new) The semiconductor chip or wafer of claim 106 further comprising a solder bump on said second contact pad..

116. (new) The semiconductor chip or wafer of claim 106 further comprising a topmost polymer layer over said passivation layer, wherein said upper metallization structure comprises an upper metal layer over said topmost polymer layer.

117. (new) The semiconductor chip or wafer of claim 106, wherein said interconnecting metallization structure comprises electroplated copper.

118. (new) The semiconductor chip or wafer of claim 106, wherein said interconnecting metallization structure comprises aluminum.

119. (new) The semiconductor chip or wafer of claim 106, wherein said gold layer is formed using a process comprising electroplating.

120. (new) A semiconductor chip or wafer comprising:

a semiconductor substrate having multiple semiconductor devices;

an interconnecting metallization structure over said semiconductor substrate and comprising a contact point;

a passivation layer over said interconnecting metallization structure, wherein said contact point is exposed by an opening in said passivation layer; and

an upper metallization structure over said contact point, wherein said upper metallization structure comprises a contact pad comprising a gold layer with a thickness of

between 2 and 100 μm and connected to said contact point, and wherein said contact pad is used to be wirebonded thereto or has a metal bump formed thereon.

121. (new) The semiconductor chip or wafer of claim 120, wherein said contact point comprises aluminum.

122. (new) The semiconductor chip or wafer of claim 120, wherein said contact point comprises electroplated copper.

123. (new) The semiconductor chip or wafer of claim 120 further comprising a topmost polymer layer over said passivation layer, wherein said upper metallization structure comprises an upper metal layer over said topmost polymer layer.

124. (new) The semiconductor chip or wafer of claim 120, wherein said interconnecting metallization structure comprises electroplated copper.

125. (new) The semiconductor chip or wafer of claim 120, wherein said interconnecting metallization structure comprises aluminum.

126. (new) The semiconductor chip or wafer of claim 120, wherein said passivation layer comprises a topmost nitride layer of said semiconductor chip or wafer.

127. (new) The semiconductor chip or wafer of claim 120, wherein said passivation layer comprises a topmost oxide layer of said semiconductor chip or wafer.

128. (new) The semiconductor chip or wafer of claim 120, wherein said passivation layer comprises a topmost insulation layer, formed using a CVD process, of said semiconductor chip or wafer.

129. (new) The semiconductor chip or wafer of claim 120, wherein said gold layer is formed using a process comprising electroplating.

130. (new) The semiconductor chip or wafer of claim 120, wherein said metal bump comprises solder.

131. (new) The semiconductor chip or wafer of claim 120 further comprising a wirebond connected to said contact pad.